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lel\$1) with ((capacitance or ،USPAT; US-PGPUB; EPO; JPO; DERWENT; US-PGPUB; EPO; JPO; DERWENT;	USPAT; US-PGPUB; EPO; JPO;	ading edge") USPAT; US-PGPUB; EPO; JPO; DERWENT	US-PGPUB: EPO: JPO: DERWENT: JBM .	US-PGPUB EPO; JPO; DERWENT; JBM -	Signal of USPAT, US-PGPUB; EPO; JPO; DERWENT;	USPAT; US-PGPUB; EPO; JPO; DERWENT;	US-PGPUB; EPO; JPO; DERWENT;	USPAT; US-PGPUB; EPO; JPO; DERWENT;	ulat\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT;	CONDATATION DO DE DE DO DE DE DE DE LOS DE DESTRENTATIONS DE DESTR	LIS BOBLIB: EBO: JBO: DERWENT;	LIS BOBLIB: FRO; JPO; DERWENT; IBM	US-PGPUB; EPO; JPO; DERWENT;	US-PGPUB; EPO; JPO; DERWENT;	EPO; JPO; DERWENT;	US-PGPUB; EPO; JPO; DERWENT;	USPAT, US-PGPUB, EPO, JPO, DERWENT, IBM TDB	O.	((((microprocessor or microcomputer or CPU or (processing adj unit)) with (power near2 (circuit\$1 or system\$1))) or ((anti-resonance near2 (circuit\$1 or system\$1))) or ((anti-resonance near2 (circuit\$1 or system\$1))) or ((anti-resonance near2) (circuit\$1 or system\$2)))	USPAT: US-PGPUB: FPO: IPO: DEBIMENT: IBM TOB	system\$1) with (model\$3 or simulat\$3))) and (resistor\$1 with (model\$3 or simulat\$3) with	(circuit\$1 or system\$1))) or //anti-resonance near2 /circuit\$1 or system\$1))) or //anti-resonance near2 /circuit\$1 or system\$1)))	((((microprocessor of microcomputer or CPU or (processing adj unit)) with (power near2 (circu USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	((((microprocessor or microcomputer or CPU or (processing adj unit)) with (power near2 (circu USPAT, US-PGPUB, EPO: JPO: DERWENT: IBM_TDB	((((microprocessor or microcomputer or CPU or (processing adjunit)) with (power near2 (circu USPAT: US-PGPUB: EPO: JPO: DERWENT: JPM_TDB	בהאשתאודי	III OSFAT, OS-FGPUB, EPO, JPO, DERWENT,	EPO; JPO; DERWENT;	Databases	·	EAST SEARCH

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DEVICE AND METHOD FOR SIMULATING ELECTRIC CIRCUIT Voltage-Controlled Oscillator.	VEHICLE SUBSYSTEM MONITORS	Adaptive transistor drive circuit	Electronically reconfigurable digital pad attenuator using segmented field effect transistors	Simulation model generation from a physical data base of a combinatorial circuit	Optoelectronic sensory neural network	Method and apparatus for testing analogue circuits	Layout pattern verification system	System for calculating and displaying user-defined output parameters describing behavior of st	Transistor-level timing and power simulator and power analyzer	Method to assess electromigration and hot electron reliability for microprocessors	Analysis mechanism for system performance simulator	Transistor-level timing and simulator and power analyzer	Device and method for calculating delay time	Method and apparatus for generating instruction/data streams employed to verify hardware im	Vehicle turn signal control system and method	Model for taking into account gate resistance induced propagation delay
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US 6501328 B US 20020143509 A US 6396316 B	US 6192739 B1 US 6116080 A	US 6279379 B1 US 6199423 B1	US 6456107 B1 V	US 6571184 B2 V	US 6781355 B2	US 20040056103 A1
US 6501328 B Power supply resonance compensation system for printed circuit board system, has damping (US 6501328 B Power supply noise reduction method for delay locked loop power supply system, involves con US 20020143509 A Power supply resonance circuit modeling apparatus used in computer, has transistor and capacitor conn US 6396316 B Buffer circuit for use in computer system specifies inductance and capacitance values of LC cir	Apparatus and methods for performing acoustical measurements Apparatus and methods for performing acoustical measurements	Apparatus and methods for performing acoustical measurements Apparatus and methods for performing acoustical measurements	US 6456107 B1 CMOS-microprocessor chip and package anti-resonance method US 6441640 B1 CMOS-microprocessor chip and package anti-resonance pass-band shunt apparatus	US 6571184 B2 System and method for determining the decoupling capacitors for power distribution systems v US 6483341 B2 CMOS-microprocessor chip and package anti-resonance apparatus	US 6781355 B2 V I/O power supply resonance compensation technique	sun microsystems and ((resonance or anti-resonance) near2 circuit): Check for double pat US 20040056103 A1/Arrangement for registration US 6842351 B2 1/Method and apparatus for I/O resonance compensation
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